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[NON-VOLATILE MEMORY AND FABRICATION THEREOF]

Abstract

A method for fabricating a non-volatile memory having two bits per cell is described. In the method, a substrate having a gate dielectric layer and a linear conductor thereon is provided, and a trapping layer is formed on the substrate and two sidewalls of the linear conductor. Two conductive spacers are then formed on the two sidewalls of the linear conductor, interposed by the trapping layer. The linear conductor will be defined into a gate, with two patterned conductive spacers on the two sidewalls thereof. The trapping layer under the two patterned conductive spacers serves as two data storage sites.